IN THE CLAIMS:

Please amend the claims as follows:

Claim 1 (Original): A data transfer method for a digital image processing apparatus, comprising the steps of:

converting first binary voltage data of n-bit (n is an integer equal to or larger than two) to multi-value current data of 2^n values;

transferring the multi-value current data through a single data line;

converting the multi-value current data on the data line to binary current data of (2^n-1) bits;

converting the binary current data of the (2^n-1) bits to second binary voltage data of (2^n-1) bits; and

restoring the first binary voltage data of the n bits from the second binary voltage data of the (2^n-1) bits.

Claim 2 (Currently Amended): A data transfer circuit for a digital image processing apparatus, comprising:

a voltage/current converter circuit for converting first binary voltage data of n-bit (n is an integer equal to or larger than two) to multi-value current data of 2^n values;

a single data transfer line for transferring the multi-value current data;

a current comparator circuit for converting the multi-value current data on the data line to binary current data of (2^n-1) bits;

a current/voltage converter circuit for converting the binary current data of the (2^n-1) bits to second binary voltage data of (2^n-1) bits; and

a counter circuit for restoring the first binary voltage data of the n bits from the second binary voltage data of the (2^n-1) bits.

Claim 3 (Original): A data transfer circuit according to claim 2, wherein:

said voltage/current converter circuit generates a current proportional to a value 2^i (i is an integer equal to or larger than zero and equal to or smaller than n-1) corresponding to each bit of the n bits, and multiplexes the generated currents to output the multi-value current data of the 2n bits having a current value proportional to the first binary voltage data of the n bits on the data transfer line.

Claim 4 (Original): A data transfer circuit according to claim 2 or 3, wherein:

said current comparator circuit expands the multi-value current data to (2n-1) bits, and outputs the binary current data of the (2^n-1) bits, the logical values of which are determined based on whether or not a current value of the multi-value current data is larger than a corresponding threshold current at each of the (2^n-1) bits.

Claim 5 (Currently Amended): A data transfer circuit according to claim 2 or 3 ~~any of claims 2 to 4~~, wherein:

said current/voltage converter circuit converts the binary current data of the (2^n-1) bits to the second binary voltage data of the (2^n-1) bits in units of bits.

Claim 6 (Currently Amended): A data transfer circuit according to claim 2 or 3 ~~any of claims 2 to 5~~, wherein:

said counter circuit comprises a logic circuit which receives the second binary voltage data of the (2^n-1) bits, and restores the first binary voltage data based on positions of bits which have logical "1."

Claim 7 (Currently Amended): A data transfer circuit according to claim 3, wherein:

said voltage/current converter circuit comprises a group of first circuits arranged in parallel in correspondence to the n bits, and

each of said first circuits generates a current proportional to ~~a~~ the value 2^i (i is an integer equal to or larger than zero and equal to or smaller than n-1) corresponding to a corresponding bit of the n bits.

Claim 8 (Original): A data transfer circuit according to claim 7, wherein:

each of said first circuits comprises:

a first transistor having a source terminal connected to a power supply terminal or a ground terminal, and a gate terminal and a drain terminal connected to each other;

a second transistor applied at a gate with first binary voltage data of the corresponding bit of the n bits from the outside, and having a drain terminal connected to the drain terminal of the first transistor; and

a third transistor having a source terminal connected to the power supply terminal or the ground terminal, and a gate terminal connected to the gate terminal of said first transistor,

said voltage/current converter circuit further comprises a first constant current source connected between the source terminal of said second transistor in each of said first circuits and the ground terminal or the power supply terminal, and

said third transistor in each of said first circuits has a drain terminal connected to the data transfer line in common.

Claim 9 (Currently Amended): A data transfer circuit according to claim 8, wherein:

said third transistor in each of said first circuits has the gate terminal, the size of which is set to have an output current value proportional to the value 2^i in accordance with the first binary voltage data of n bits supplied from the outside.

Claim 10 (Original): A data transfer circuit according to claim 4, wherein:

said current comparator circuit comprises a group of second circuits arranged in parallel in correspondence to the (2^n-1) bits, and

each of said second circuits sets a logical value of a corresponding bit to "1" when a current value of the multi-value current data is larger than a corresponding threshold current.

Claim 11 (Original): A data transfer circuit according to claim 10, wherein:

said current comparator circuit comprises a fourth transistor which receives the multi-value current data at a drain, and has a gate terminal connected to the drain terminal, and a source terminal connected to a ground terminal or a power supply terminal, and said group of second circuits, and

each of said second circuits comprises:

a fifth transistor having a gate terminal connected to the gate terminal of said fourth transistor, a source terminal connected to a common ground terminal or a common power supply terminal; and

a second constant current source connected between the drain terminal of said fifth transistor and the power supply terminal or the ground terminal for applying the threshold current, and

said current comparator circuit outputs the second binary current data of the (2^n-1) bits, the logical value of which is set to "1" from LSB to a bit corresponding to the threshold current.

Claim 12 (Original): A data transfer circuit according to claim 11, wherein:

said second constant current source applies different threshold currents of the (2^n-1) bits in predetermined step units, and

said current comparator circuit outputs binary current data of (2^n-1) bits which has a bit corresponding to the largest threshold current at MBS, and a bit corresponding to the smallest threshold current at LSB.

Claim 13 (Original): A data transfer circuit according to claim 5, wherein:

said current/voltage converter circuit comprises a group of third circuits arranged in parallel in correspondence to the (2^n-1) bits of the binary current data, respectively, and

each of the third circuits converts a corresponding bit of the binary current data of the (2^n-1) bits to a corresponding bit of the second binary voltage data of (2^n-1) bits.

Claim 14 (Original): A data transfer circuit according to claim 13, wherein:

said current/voltage converter circuit comprises a third constant current source and said group of third circuits, and

each of said third circuits comprises:

a sixth transistor having a source terminal connected to a common power supply terminal or a common ground terminal, and a gate terminal connected to a drain terminal; and

a seventh transistor having a gate terminal for receiving the binary current data of a corresponding bit of the (2^n-1) bits, a source terminal connected to said third constant current source, and a drain terminal connected to the drain terminal of said sixth transistor.

Claim 15 (Original): A data transfer circuit according to claim 6, wherein:

said counter circuit comprises a logic circuit for restoring the first binary voltage data of the n bits which have all bits at logical "0" when all the bits of the second binary voltage data of the (2^n-1) bits are logical "0," and restoring the first binary voltage data of the n bits corresponding to a binary number of the number of bits of logical "1" from LSB of the second binary voltage data of the (2^n-1) bits.

Claim 16 (Original): A data transfer circuit according to claim 15, wherein:

said counter circuit comprises a bit determination circuit for three least significant bits, and

said bit determination circuit comprises:

a first 3-bit input AND circuit for outputting logical "1" when the three least significant bits are logical "1";

a second 3-bit input AND circuit for outputting logical "1" when only a third bit is logical "1"; and

an OR circuit for calculating a logical OR of the output of said first 3-bit input AND circuit and the output of said second 3-bit input AND circuit.

Claims 17-30 (Canceled).

Claim 31 (New): A data transfer circuit according to claim 4, wherein:

said current/voltage converter circuit converts the binary current data of the (2^n-1) bits to the second binary voltage data of the (2^n-1) bits in units of bits.

Claim 32 (New): A data transfer circuit according to claim 4, wherein:

said counter circuit comprises a logic circuit which receives the second binary voltage data of the (2^n-1) bits, and restores the first binary voltage data based on positions of bits which have logical "1."

Claim 33 (New): A data transfer circuit according to claim 5, wherein:

said counter circuit comprises a logic circuit which receives the second binary voltage data of the (2^n-1) bits, and restores the first binary voltage data based on positions of bits which have logical "1."